

REMARKS

Favorable reconsideration of this application, in light of the following discussion and in view of the present amendment, is respectfully requested.

Claims 1, 6-8, 15-16, 19-21 have been amended. Claims 2-3 have been cancelled. New claims 28 and 29 have been added. Claims 1 and 4-29 are pending and under consideration.

I. Rejections under 35 U.S.C. § 103

In the Office Action, at pages 4-10, numbered paragraphs 8-28, claims 1, 4, 6-12, 15-17, and 19-25 were rejected under 35 USC § 103(a) as being unpatentable over Yamada (U.S. Patent No. 5,950,222) in view of Iwata (U.S. Patent No. 5,881,295).

Neither Yamada nor Iwata discusses or suggests "a conversion circuit that includes a plurality of registers to which a plurality of addresses indicating respective storage places of the alternate interrupt vectors are set, and that, based on a state of the flag, converts a first address indicating a storage place of the interrupt vector that is accessed by the central processing unit into a second address indicating a storage place of the corresponding alternate interrupt vector by outputting the second address from one of the registers corresponding to the first address," as recited in independent claim 1 as amended. The Examiner concedes that Yamada does not disclose a conversion circuit and seeks to make up for this deficiency with reference to the address conversion circuit of Iwata (Iwata, col. 14, lines 6-15; Fig. 5). However, the address conversion circuit of Iwata does not include a register, much less a plurality of registers, as is recited in amended claim 1.

Further, it would not have been obvious to modify the microcomputer of Yamada with the data processor of Iwata to improve the safety of a system during on-board programming of a program memory or to provide additional safety by preventing a microcomputer from running away and from being damaged even when an interrupt handling or exception handling is requested during on-board programming of the program memory. There is no adequate motivation to combine the microcomputer of Yamada with the data processor of Iwata without having to rely on the Applicant's own disclosure and, even if Yamada were combined with Iwata, the claimed invention would not result. Therefore, amended claim 1 patentably distinguishes over the references relied upon. Accordingly, withdrawal of the § 103(a) rejection is respectfully requested.

For reasons similar to those discussed above, neither Yamada nor Iwata discusses or suggests "a conversion circuit that includes a first pair of registers for setting a first address

range and a second pair of registers for setting a second address range, and that, when an address within the first range is accessed by the central processing unit, performs address conversion based on a state of the flag to convert the first address range to the second address range,” as recited in independent claim 15 as amended. Again, the address conversion circuit of lwata does not include a register, much less a first pair of registers and a second pair of registers, as is recited in amended claim 15. Therefore, amended claim 15 patentably distinguishes over the references relied upon. Accordingly, withdrawal of the § 103(a) rejection is respectfully requested.

Claims 4-14 and 16-27 depend either directly or indirectly from amended claims 1 and 15, respectively, and include all the features of claims 1 and 15, plus additional features that are not discussed or suggested by the references relied upon. Therefore, claims 4-14 and 16-27 patentably distinguish over the references relied upon for at least the reasons noted above. Accordingly, withdrawal of these § 103(a) rejections is respectfully requested.

II. Rejections under 35 U.S.C. § 112

In the Office Action, at pages 3-4, numbered paragraphs 6-7, claims 2-3 were rejected under the second paragraph of 35 USC § 112 as being indefinite. Claims 2-3 have been cancelled. Accordingly, withdrawal of the § 112 rejections is respectfully requested.

III. Objection to the Specification

In the Office Action, at page 3, numbered paragraph 5, the title of the invention was objected as not descriptive. As per the Examiner’s suggestion, the title of the invention was changed in response to this objection. Accordingly, withdrawal of the objection is respectfully requested.

IV. New claims

New independent claims 28 and 29 have been added. None of the prior art cited by the Examiner discusses or suggests “a conversion circuit that includes a register to which an offset is set, and that converts a first address indicating a storage place of the interrupt vector that is accessed by the central processing unit into a second address indicating a storage place of the corresponding alternate interrupt vector by adding the offset to the first address,” as recited in claim 28. Therefore, new claim 28 patentably distinguishes over the references relied upon. None of the prior art cited by the Examiner discusses or suggests “a conversion circuit that, based on a state of the flag, converts an address indicating a storage place of an interrupt vector that is accessed by the central processing unit into an address indicating a storage place of a

corresponding alternate interrupt vector," as recited in claim 29. Therefore, new claim 29 patentably distinguishes over the references relied upon. Thus, it is submitted that new claims 28 and 29 are in a condition suitable for allowance.

Conclusion

Claims 1 and 4-29 are pending and under consideration.

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

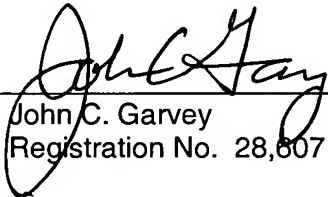
Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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